REMARKS

Claims 34-47 have been cancelled from the application, claims 1, 13, 15 and 26 are amended; new claims 48-55 are added; and claims 1-33 and 48-55 are pending in the application.

Claims 22-25 and 30-33 are indicated to contain allowable subject matter, but stand objected to for depending from rejected base claims. New claims 48-55 correspond to claims 22-25 and 30-33, respectively, amended to place the claims in independent form. New claims 48-55 are therefore believed allowable, and Applicant requests formal allowance of such claims in the Examiner's next action.

Claims 1-21 and 26-29 stand rejected as being unpatentable over Hosotani, either alone, or in combination with Prinz or Koganei. Applicant has amended claims 1, 13, 15 and 26, from which the remaining claims depend, and believes that such amendments place the claims in condition for allowance.

Referring first to claim 1, the amended claim recites a magnetoresistive memory device containing a memory bit stack which includes a first magnetic layer, a second magnetic layer, and a non-magnetic layer between the first and second magnetic layers. The amended claim further recites a first conductive line proximate the stack and configured for utilization in reading information from the memory bit, and a second conductive line spaced from the stack by a greater distance than any distance which the first conductive line is spaced from the stack, and configured for utilization in writing information to the bit. The amended claim further recites that <u>the first and second conductive lines extend longitudinally parallel to one another</u>.

The amendment to the claim introduces the limitation that the first and second conductive lines extend longitudinally parallel to one another. Such amendment is supported by the originally-filed application at, for example, Fig. 1, wherein a line utilized in reading information from a memory bit (line 18 of Fig. 1) is shown adjacent a memory bit stack (stack 20), and a line utilized in writing information to the memory bit (line 14) is shown spaced form the stack by a greater distance than the distance from which the line 18 is spaced from the stack. Further, Fig. 1 shows the line utilized for writing information to the memory bit (line 14) extending longitudinally parallel to the line utilized for reading information from the bit (line 18).

Amended claim 1 is believed allowable over the Examiner's cited references for at least the reason that the references do not suggest or disclose recited conductive line utilized for reading information from a memory bit stack being closer to the stack than the conductive line utilized in writing information from the memory bit stack, in combination with the feature that the conductive lines utilized for reading information from the stack and writing information to the memory bit stack extend longitudinally parallel to one another.

The Examiner cites Hosotani for disclosing a magnetoresistive memory device having a conductive line utilized for reading information from a memory bit closer to the memory bit than is a conductive line utilized for writing information to the memory bit. Specifically, the Examiner refers Applicant to Fig. 30A of Hosotani, and indicates that such figure shows a memory bit 25, a line 27 close to the memory bit utilized for reading information from the memory bit, and another line 29 spaced from the memory bit further than is the line 27, utilized for writing information. Applicant notes that the device shown in Fig. 30A of Hosotani is distinguishable from the device recited in amended claim 1 for at

least the reason that the line referred to by the Examiner as being utilized for writing information to the device (line 29) extends longitudinally or orthogonal to the line identified by the Examiner as being utilized for reading information from a memory bit of the device (line 27), as indicated in, for example, Fig. 12 of Hosotani. Further, Applicant notes that Hosotani does not disclose or suggest that a line utilized for writing information to a memory bit which is spaced further from the memory bit than the line utilized for reading information from the memory bit, would also extend longitudinally parallel to the line utilized for reading information from the memory bit. The subject matter of amended claim 1 is therefore not disclosed or suggested by Hosotani.

Applicant submits that the subject matter of amended claim 1 is also not disclosed or suggested by any combination of Hosotani with the Examiner's other cited references of Prinz and Koganei. Specifically, none of the Examiner's cited references suggests or discloses a magnetoresistive memory device in which a conductive line utilized for writing information from a memory bit is spaced from the memory bit by a greater distance than a conductive line utilized for reading information from the memory bit, and yet extends longitudinally parallel to the conductive line utilized for reading information from the memory bit.

Amended claim 1 is allowable over the Examiner's cited references for the reasons discussed above, and Applicant therefore requests formal allowance of amended claim 1 in the Examiner's next action. Claims 2-12 depend from claim 1, and are therefore allowable for at least the reasons discussed above regarding amended claim 1, as well as for their own recited features which are neither shown nor suggested by the cited art.

Referring next to claim 13, such claim is amended similarly to claim 1 to recite a magnetoresistive memory device comprising a memory bit, a conductive line utilized for reading information from the bit and a conductive line utilized for writing information to the bit, with the conductive line utilized for writing information to the bit being further from the bit than the line utilized for reading information from the bit and extending longitudinally parallel to the line utilized for reading information from the bit. Claim 13 is therefore allowable for reasons similar to those discussed above regarding claim 1. Accordingly, Applicant requests formal allowance of claim 13 in the Examiner's next action.

Claim 14 depends from claim 13, and is therefore allowable for at least the reasons discussed above regarding claim 13, as well as for its own recited features.

Referring next to claim 15, such recites a magnetoresistive memory device in which a recited second conductive line is under a stack comprising first and second magnetic layers, and configured to generate an electrical field which overlaps at least a portion of the stack to alter a magnetic orientation within at least one of the magnetic layers. The claim also recites a third conductive line spaced from the stack by a greater distance than the recited second conductive line, and configured to generate an electric field which overlaps at least a portion of the stack to alter a magnetic orientation within at least one of the magnetic layers. Additionally, the amended claim recites that the second and third conductive lines extend longitudinally parallel to one another. Amended claim 15 is allowable for reasons similar to those discussed above regarding claim 1, and Applicant therefore requests formal allowance of claim 15 in the Examiner's next action.

Claims 16-25 depend from claim 15, and are therefore allowable for at least the reasons discussed above regarding claim 15, as well as for their own recited features which are neither shown nor suggested by the cited art.

Referring next to claim 26, the amended claim recites a magnetoresistive memory device having a first conductive line extending across a set of individual memory bits and configured for utilization of reading information from the memory bits, and a second conductive line extending across the set of memory bits and spaced from the stacks of memory bits by a greater distance than any distance that the first conductive line is spaced from the stacks of memory bits. The second conductive line is recited to be configured for utilization in writing information to the memory bits. The first and second conductive lines are recited to extend longitudinally parallel to one another. Claim 26 is allowable for reasons similar to those discussed above regarding claim 1, and Applicant therefore requests formal allowance of claim 26 in the Examiner's next action.

Claims 27-33 depend from claim 26, and are therefore allowable for at least the reasons discussed above regarding claim 26, as well as for their own recited features which are neither shown nor suggested by the cited references.

Claims 1-33 are allowable for the reasons discussed above, and new claims 48-55 are believed allowable. Applicant therefore requests formal allowance of claims 1-33 and 48-55 in the Examiner's next action.

The Examiner has lodged several objections to the specification. The Examiner has asked that the title be amended. Without admission as to the propriety of the Examiner's request, Applicant has amended the title in compliance with the Examiner's request. The

Examiner has also asked that the Abstract be amended. Without admission as to the propriety of the Examiner's request, Applicant has made such amendment.

The Examiner also objects to the Brief Description of the Drawings, and indicates that Fig. 1 appears to be mislabeled, in that it is the Examiner's opinion that Fig. 1 appears to be a prior art MRAM device. Applicant respectfully submits that the Examiner is mistaken. Fig. 1 shows the conductive lines 18 and 14 of the present invention (with one of the conductive lines being utilized for reading information from a memory bit stack, and the other of the conductive lines being utilized for writing information to the memory bit stack), and accordingly is not a prior art MRAM device. Applicant therefore requests that the Examiner's objection to the description of Fig. 1 in the Brief Description of the Drawings be withdrawn in the Examiner's next action.

The Examiner objects to the specification utilizing the terms “first” and “second” in a context which appears to be opposite to that utilized in the claims. Specifically, the specification refers to the conductive line utilized for writing to a memory bit (line 14) as a “first” electrically conductive line, and refers to the conductive line 18 utilized for reading information from a memory bit as “second” electrically conductive line. Several of the Applicant’s claims, in contrast, refer to the conductive line utilized for a writing operation as being a “second” conductive line and that utilized for a reading operation as being a “first” conductive line. Applicant respectfully submits that the terms “first” and “second” are labels utilized to indicate an order of introduction of the various described features, and that it is not necessary or required that the labels be utilized identically in the specification and claims. However, in an effort to expedite prosecution of the present application, Applicant has amended the specification to indicate that the conductive line 14 is a second

conductive line, and that conductive line 18 is a first conductive line. Applicant therefore requests that the Examiner's objections to the utilization of “first” and “second” in the specification be withdrawn in the Examiner's next action.

The pending claims are allowable for the reasons discussed above, and the Examiner's objections to the specification are addressed by the comments and amendments provided herein. Applicant therefore believes that the application is now in condition for formal allowance, and requests that the Examiner's next action be a Notice of Allowance.

Respectfully submitted,

Dated: 8/4/03

By: _____
David G. Latwesen, Ph.D.
Reg. No. 38,533